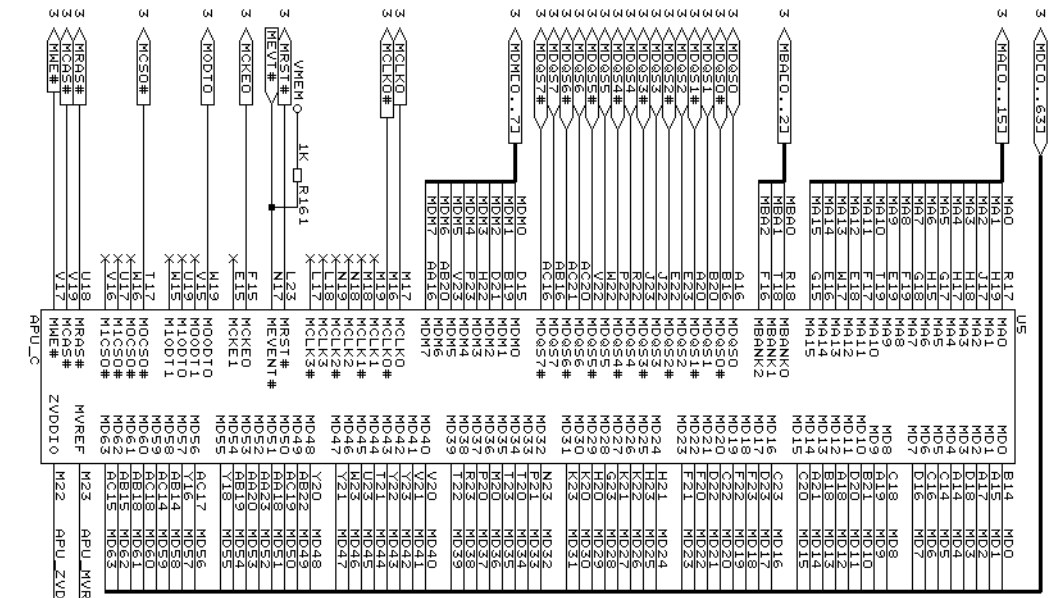
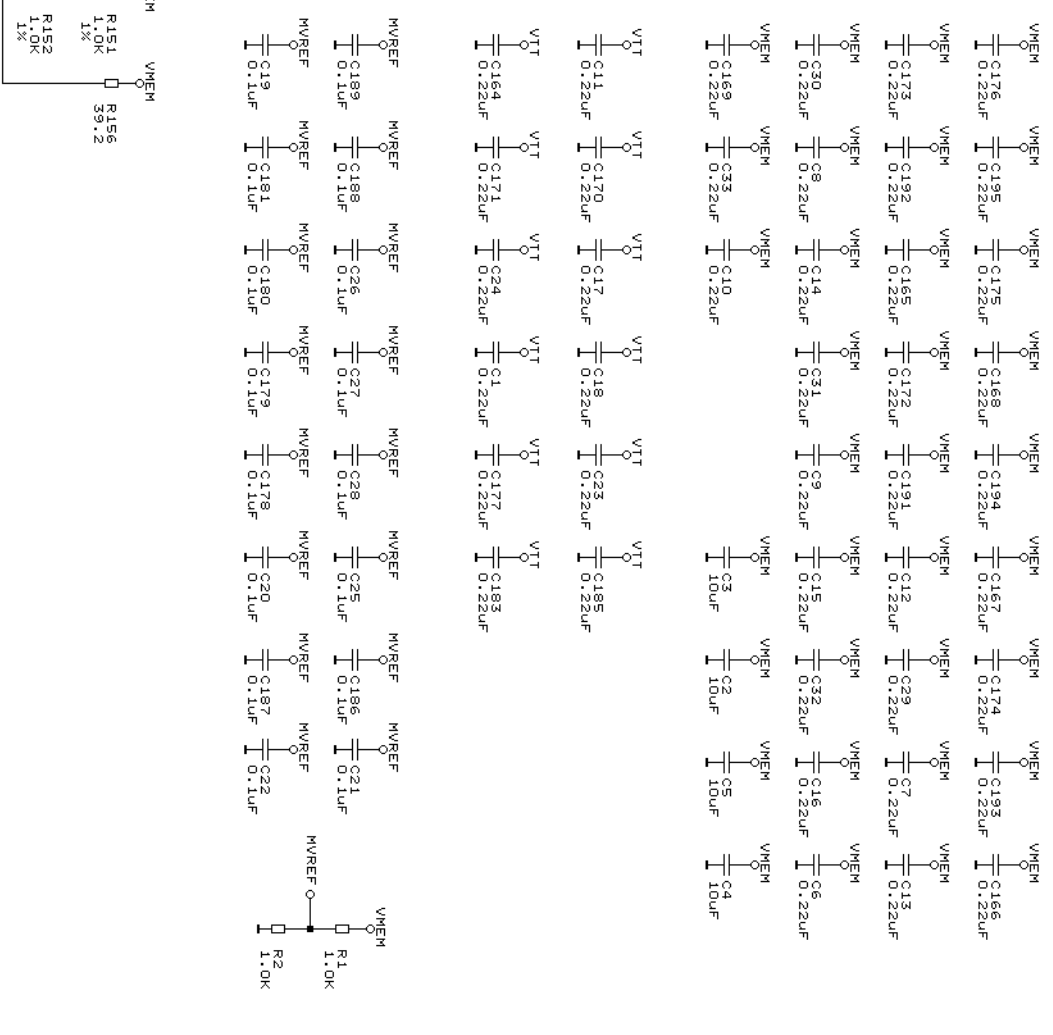
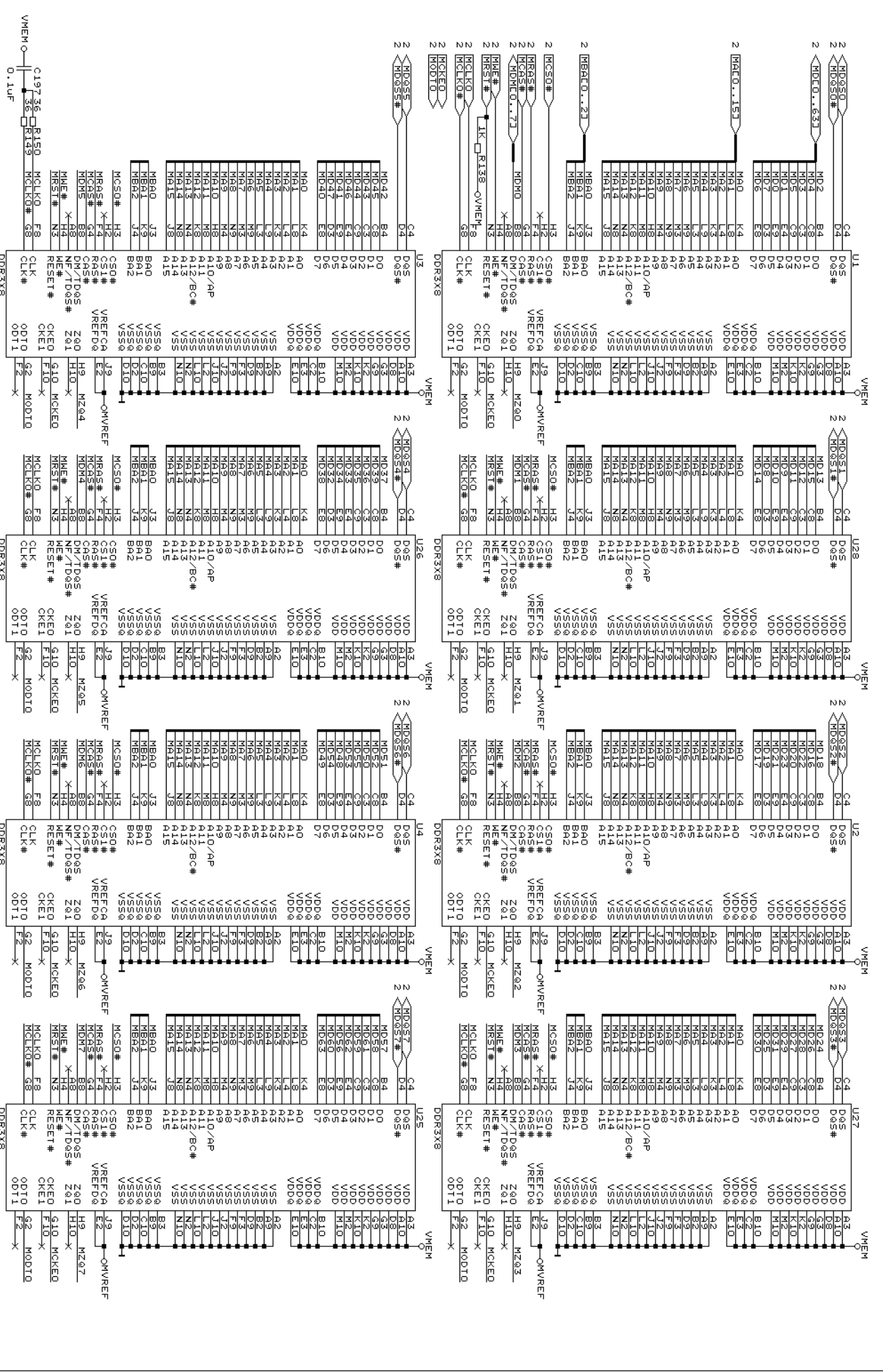


APU DRAM Interface



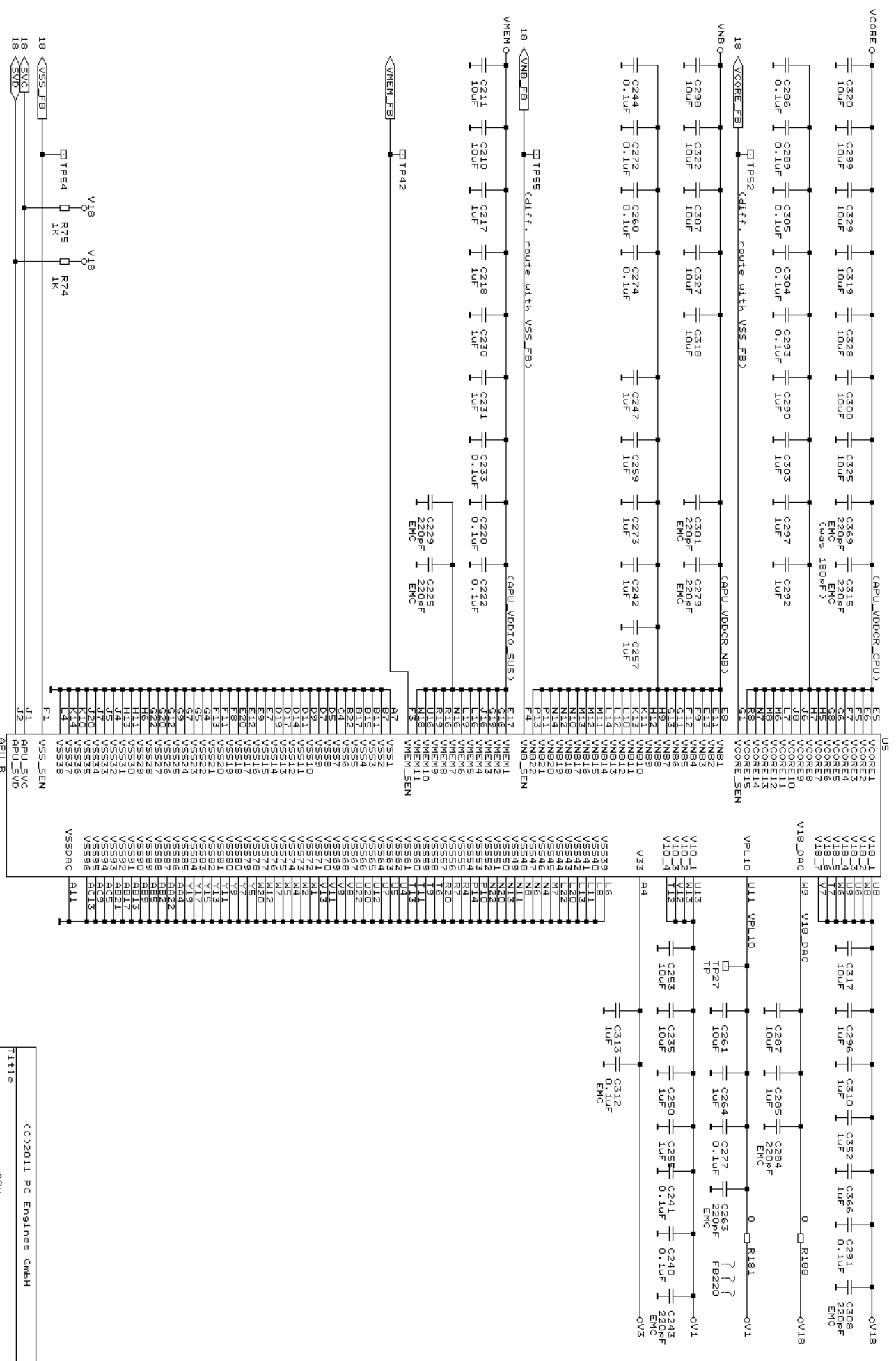
DRAM bypass





<p> Title DDR3 DRAM </p> <p> Size/Document Number apu </p> <p> Date: August 17, 2013 Sheet 3 of 18 </p>	<p> ©2011 PC Engines GmbH </p>
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APU power



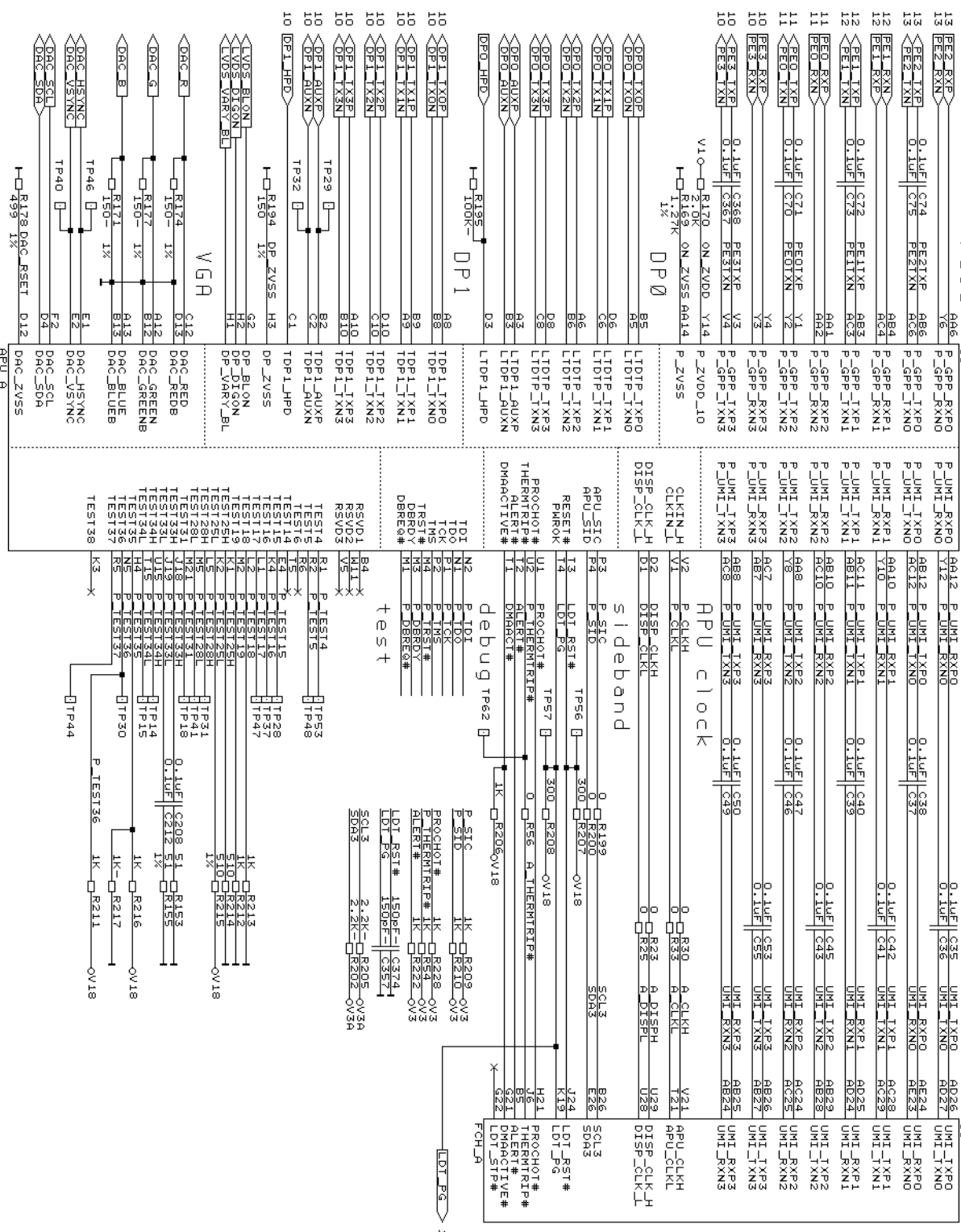
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Size/Document Number		APU power	
Date:		May 4, 2013/Sheet	
REV		4 of 18	

PCIe

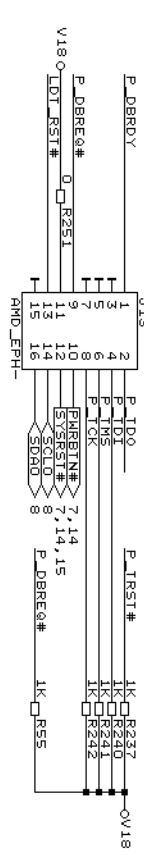
APU

UMI

FCH



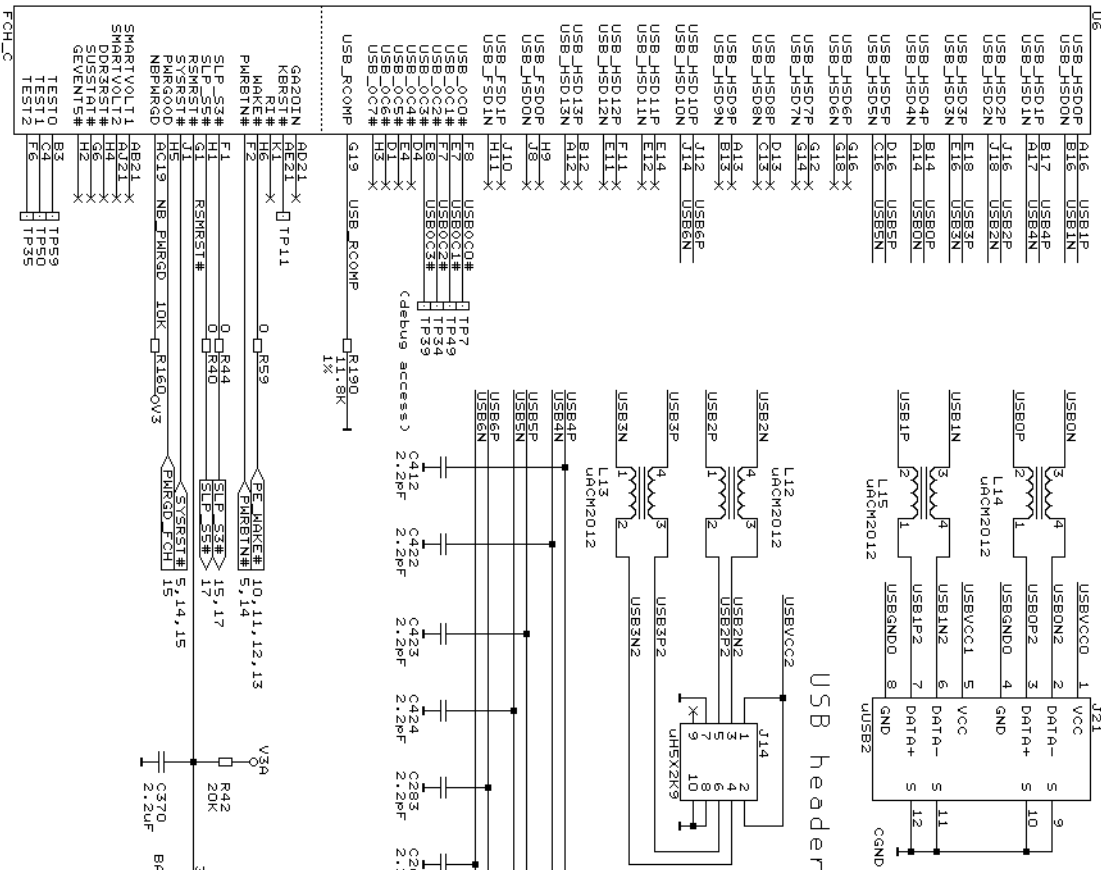
AMD embedded probe header



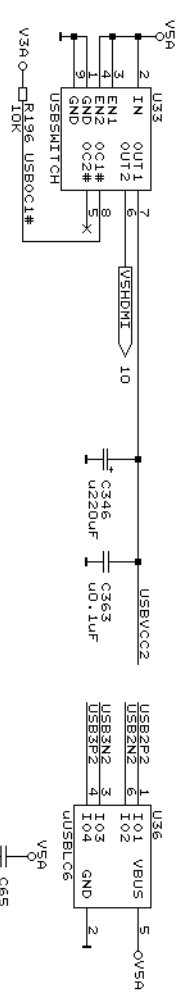
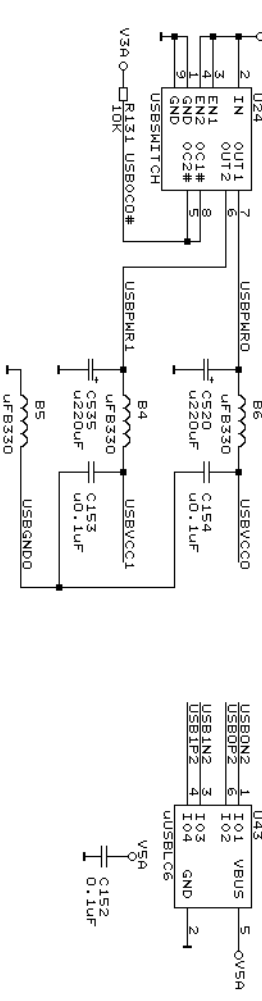
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Size/Document Number		apu	
Date/September 2, 2013/Sheet		5 of 18	
REV		1D	

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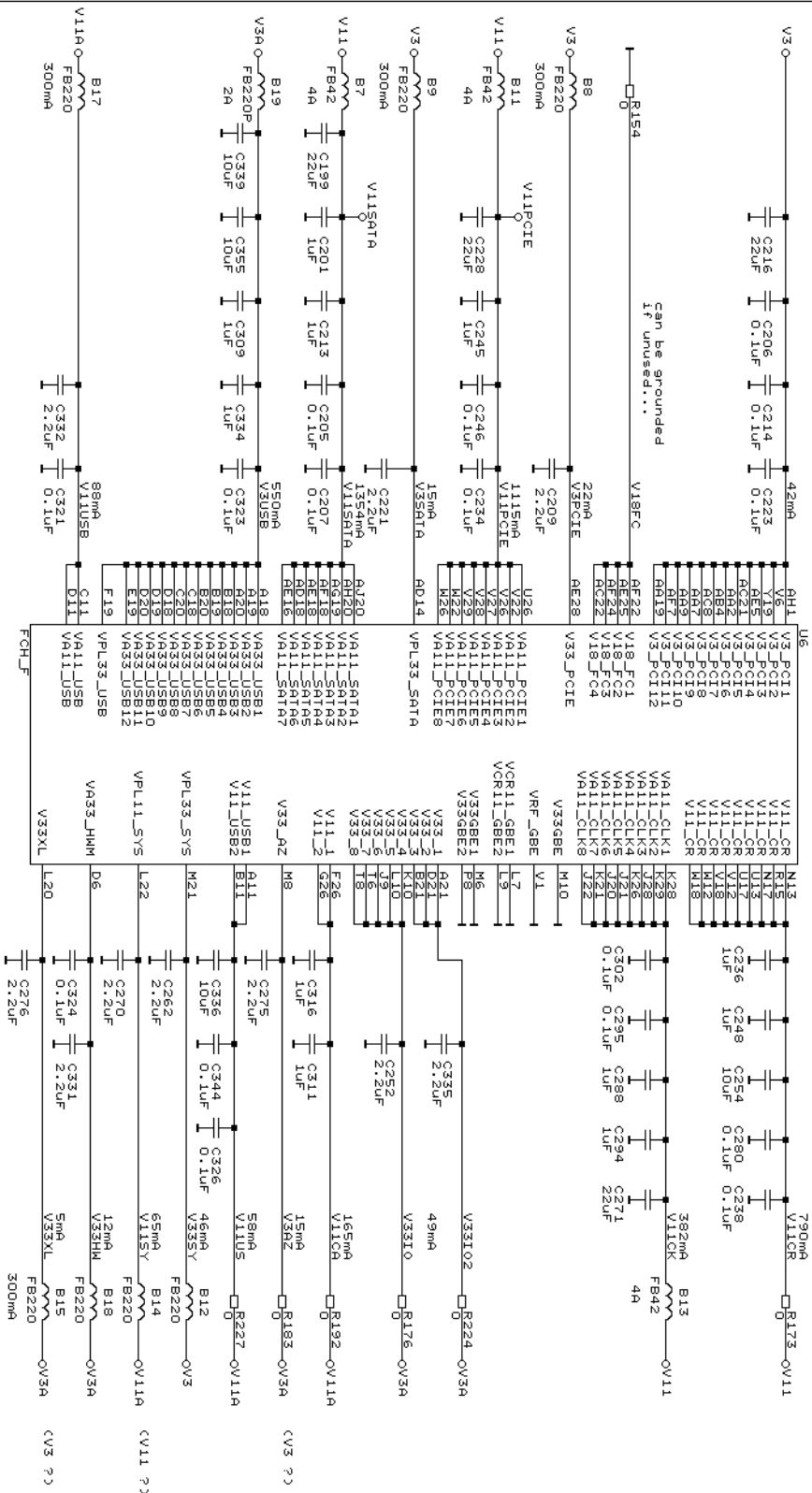
FCH USB, ACPI



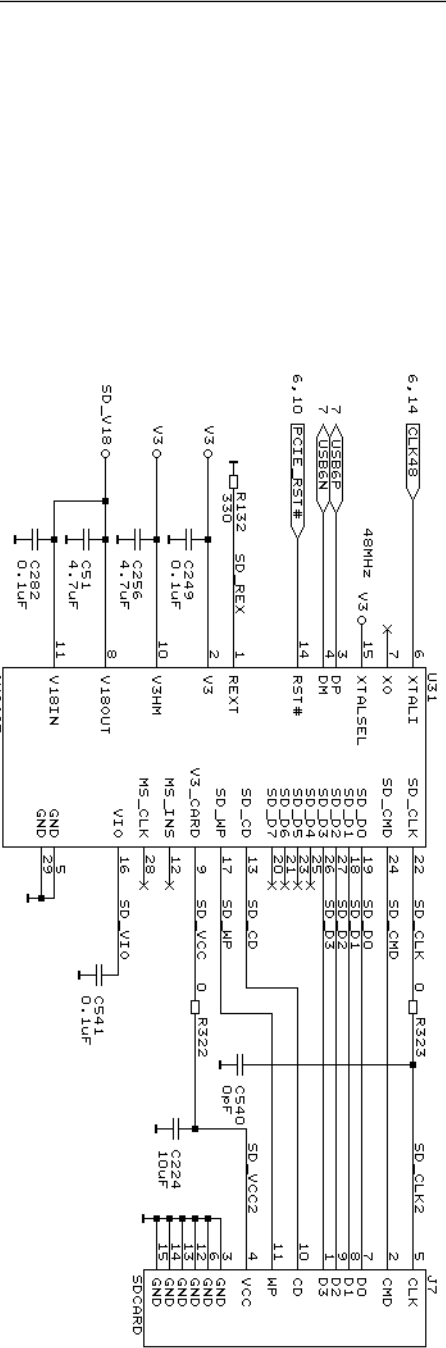
USB power

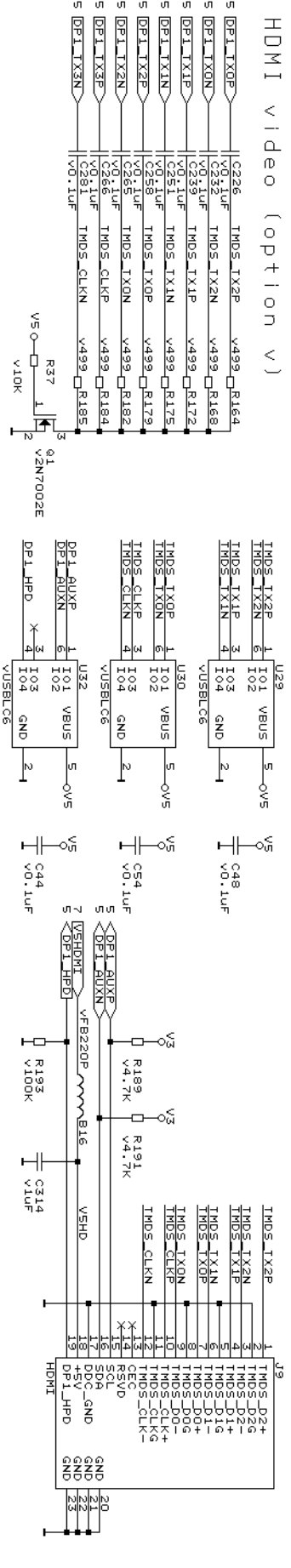


FCH power

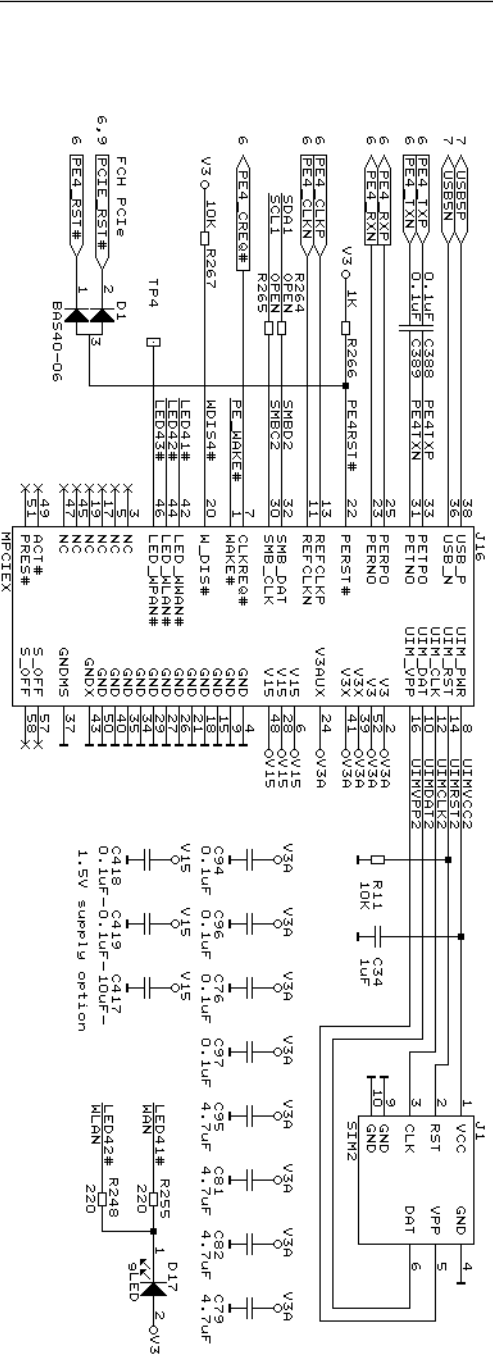
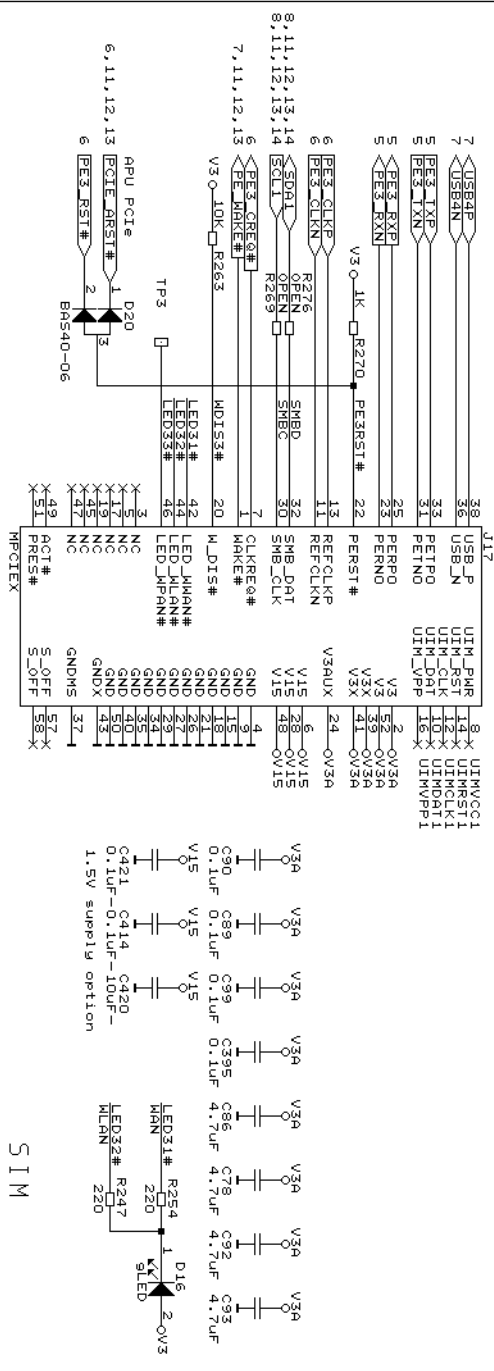


SD card interface





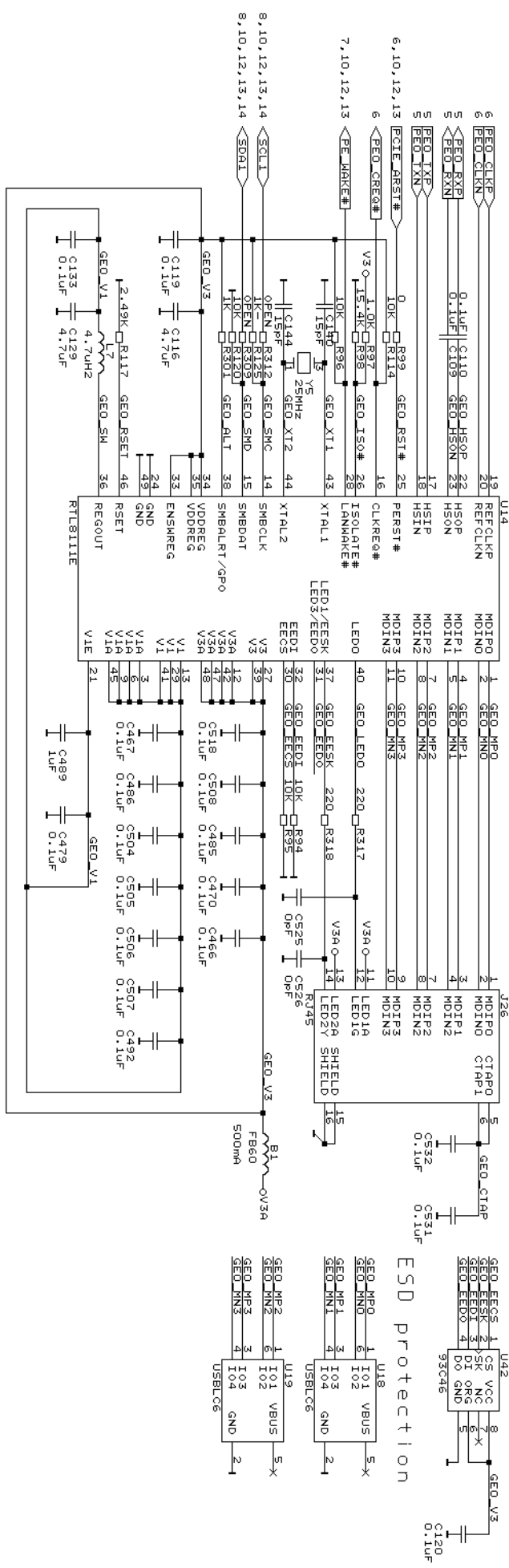
miniPCI Express



Gigabit Ethernet 1

RJ45

EEPROM

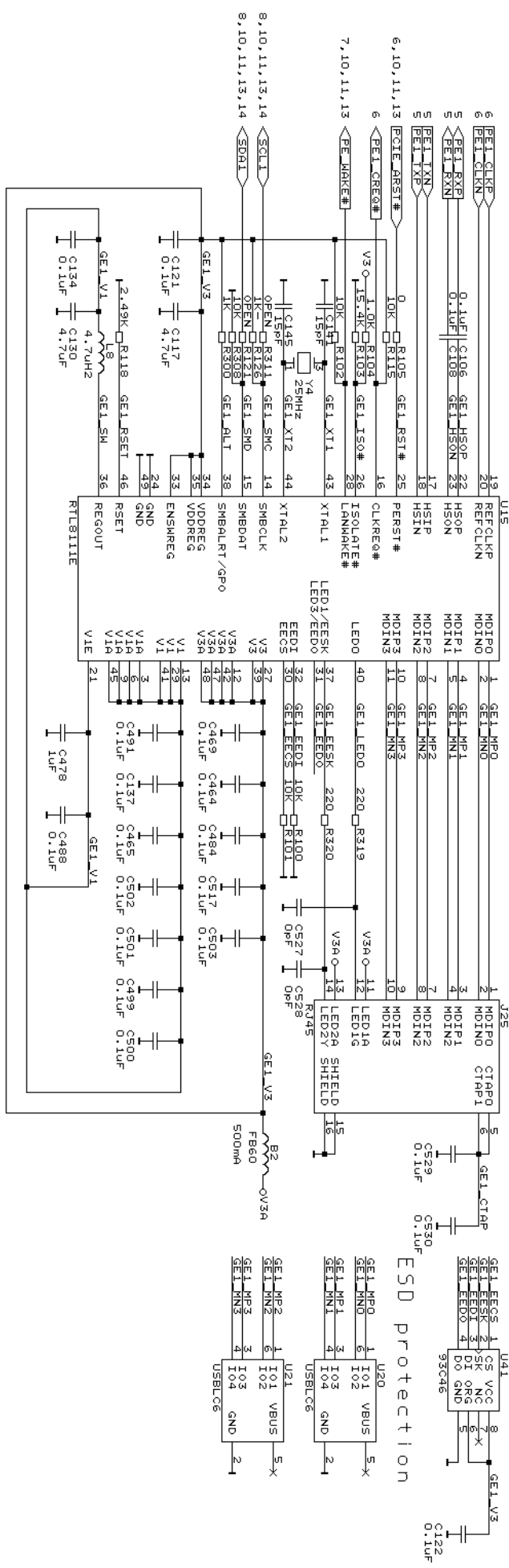


Title		Ethernet (1)	
Size/Document Number		apu	
Date		September 17, 2013	
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REV		1D	

Gigabit Ethernet 2

RJ45

EEPROM

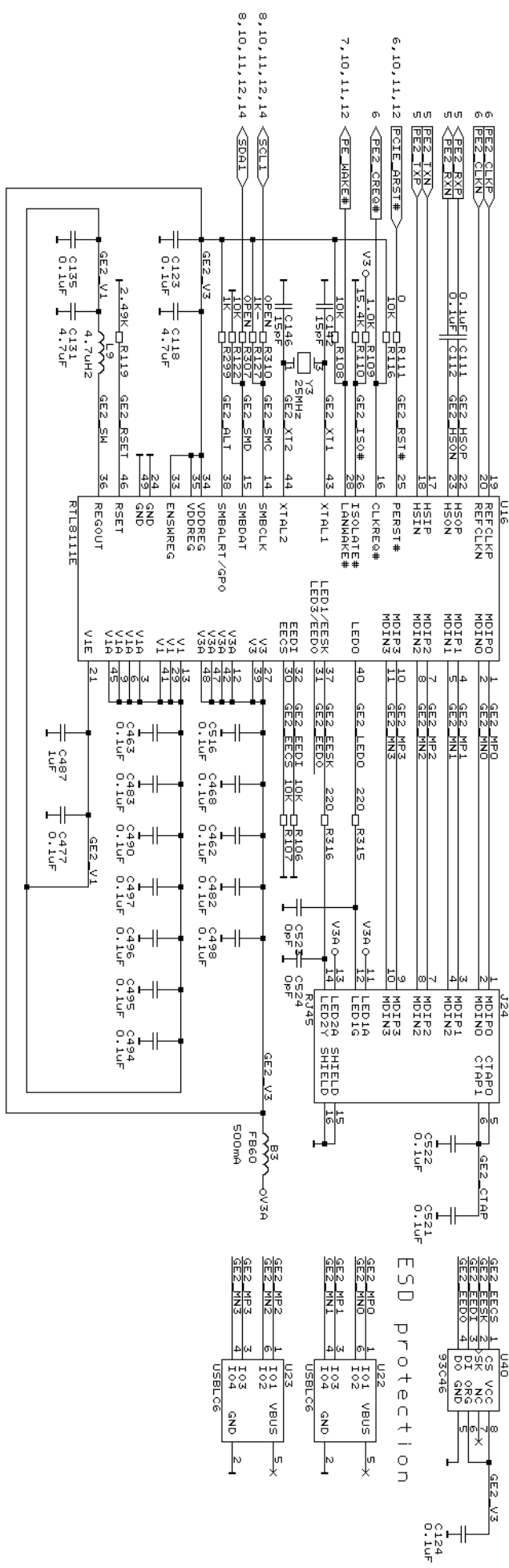


Title		Ethernet (2)	
Size/Document Number		apu	
Date		September 17, 2013	
Sheet		12 of 18	
REV		1D	
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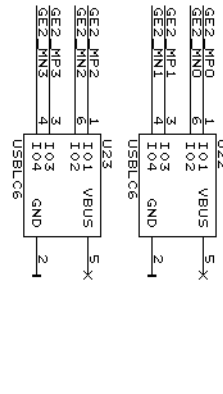
Gigabit Ethernet 3

RJ45

EEPROM

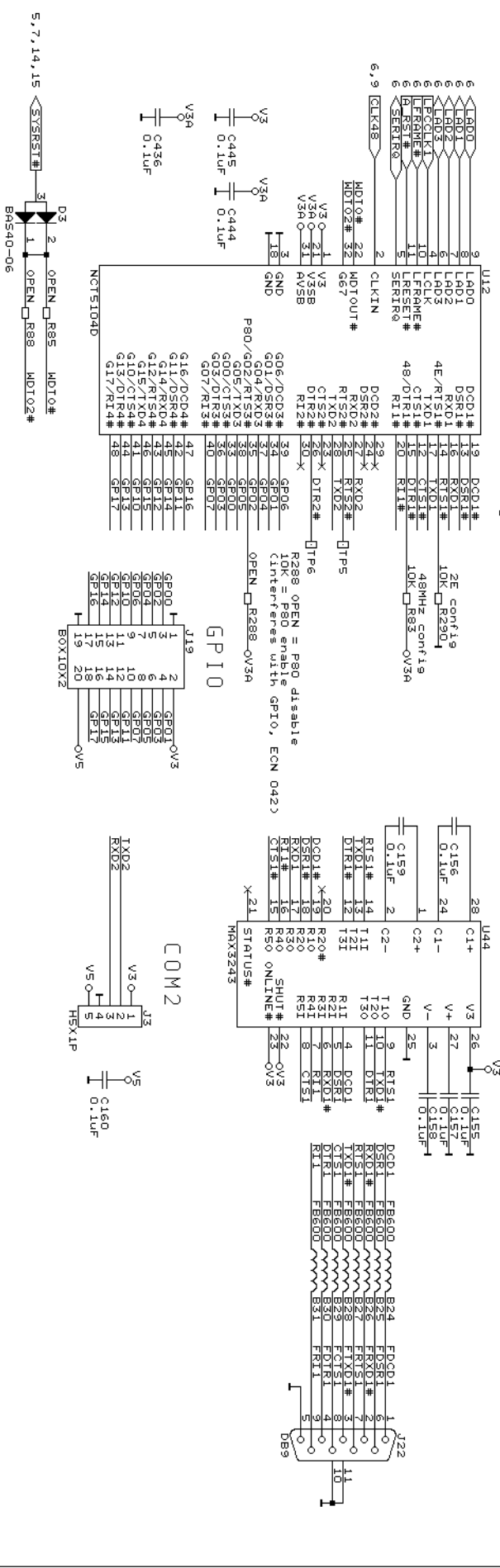


ESD protection

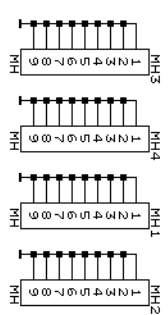


Title		Ethernet (3)	
Size/Document Number		apu	
Date		September 17, 2013	
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REV		1D	

LPC UART + watchdog



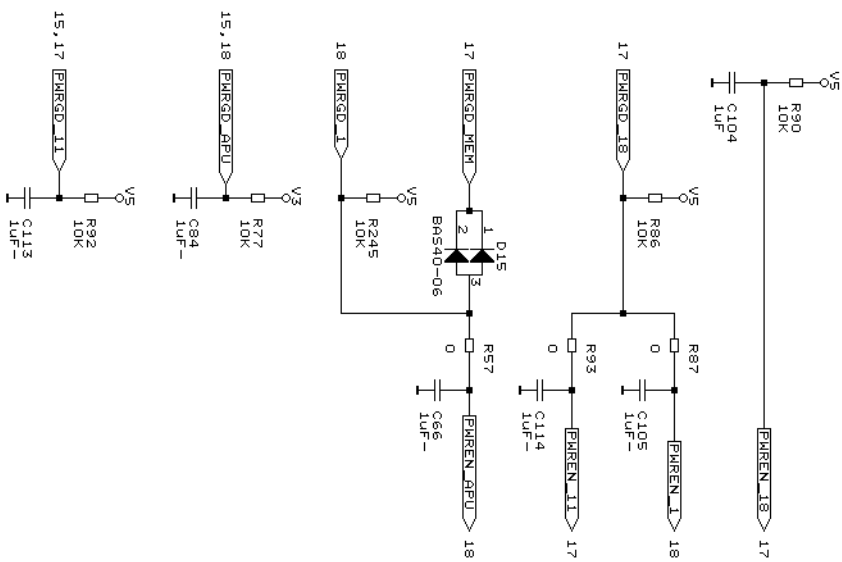
Mounting holes



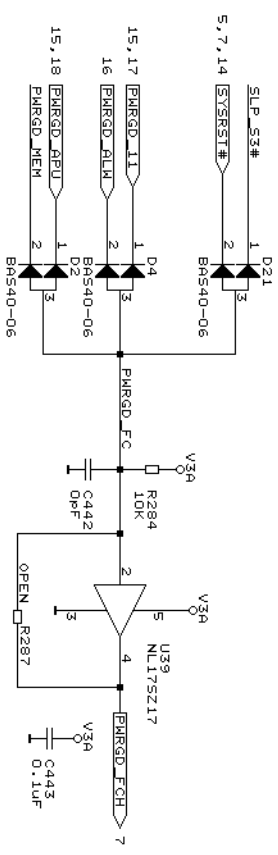
Fiducial marks

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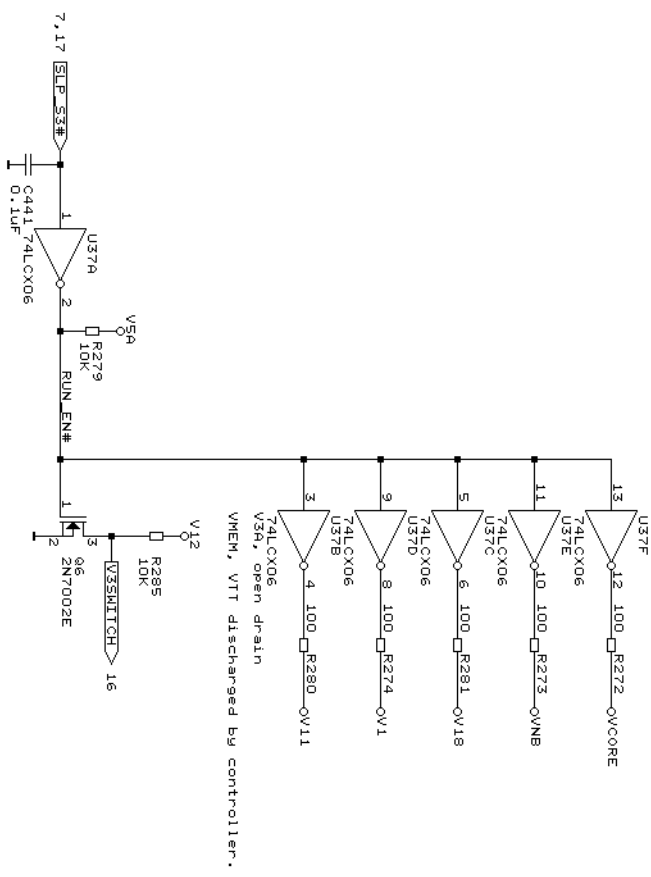
Power sequence



FCH power good



Voltage plane discharge

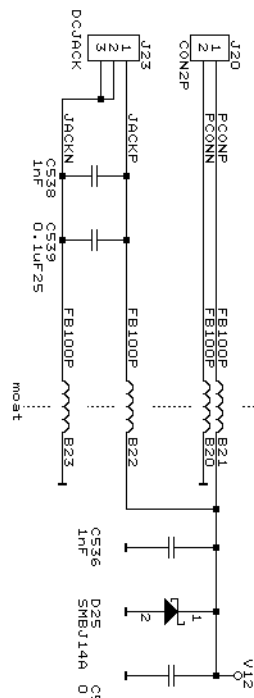


V3M1, VTT discharged by controller.

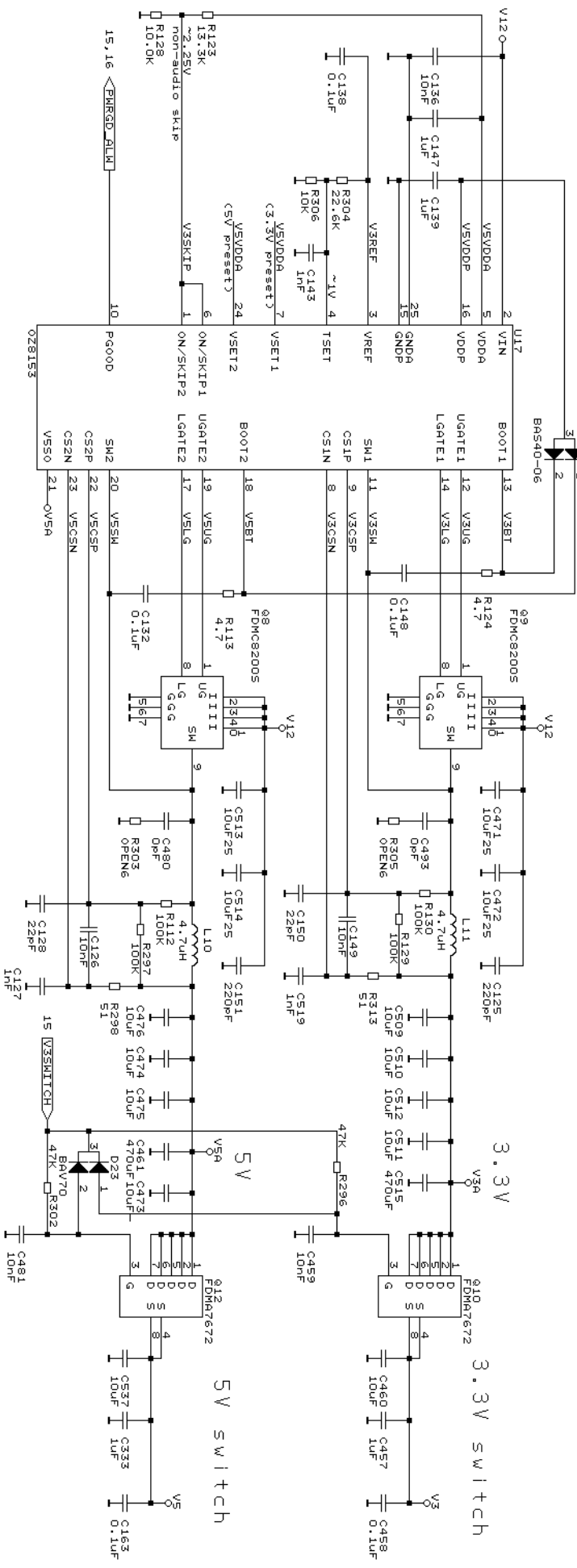
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Size		Document Number	
B	REV	apu	1D
Date: February 7, 2013		Sheet 15 of 18	

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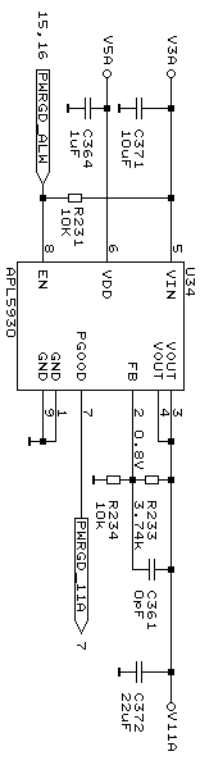
Power Input +12V



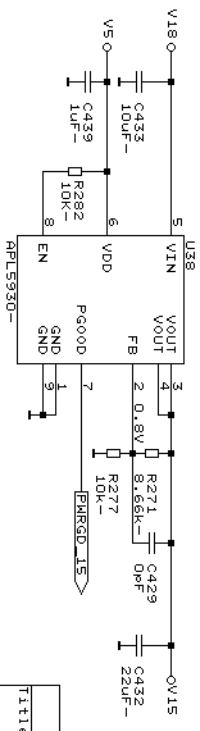
3.3V and 5V converter



3.3V always -> 1.1V LDO

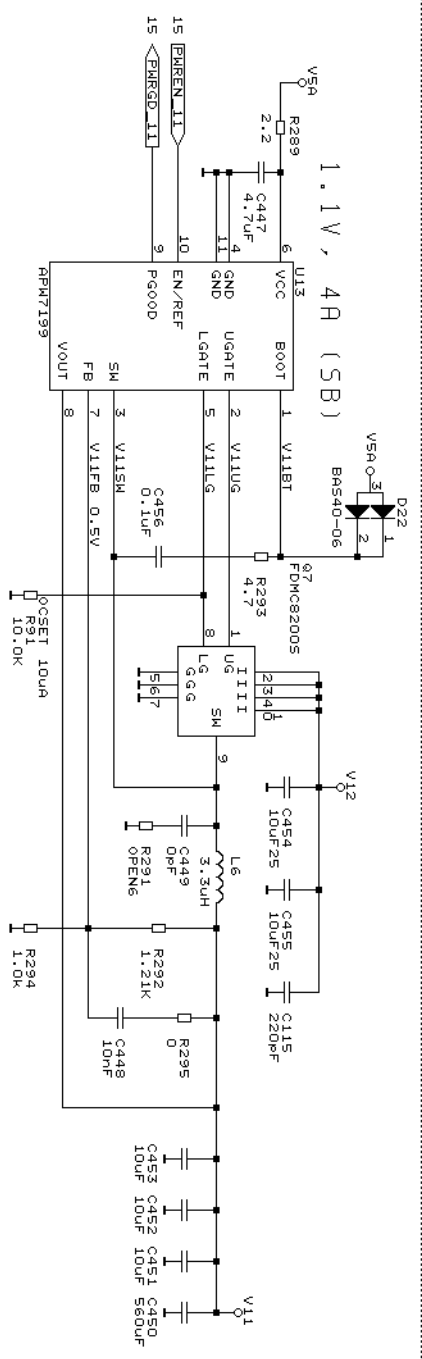
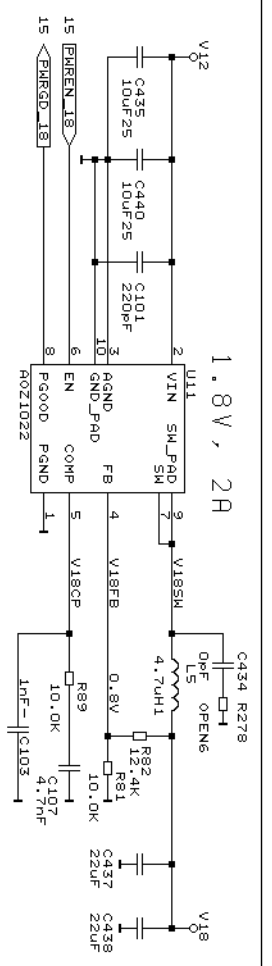


1.8V -> 1.5V LDO (option)

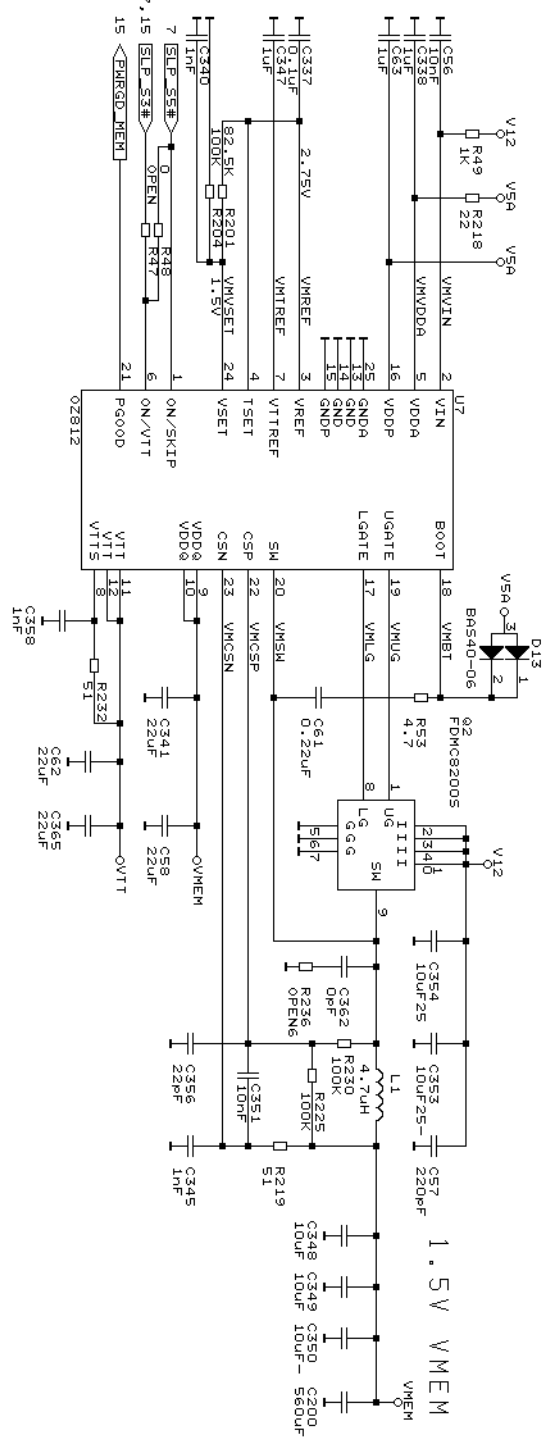


used for multiPCI express, normally not populated

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Size		Power In, 3.3V, 5V	
Document Number		apu	
Date		September 2, 2013	
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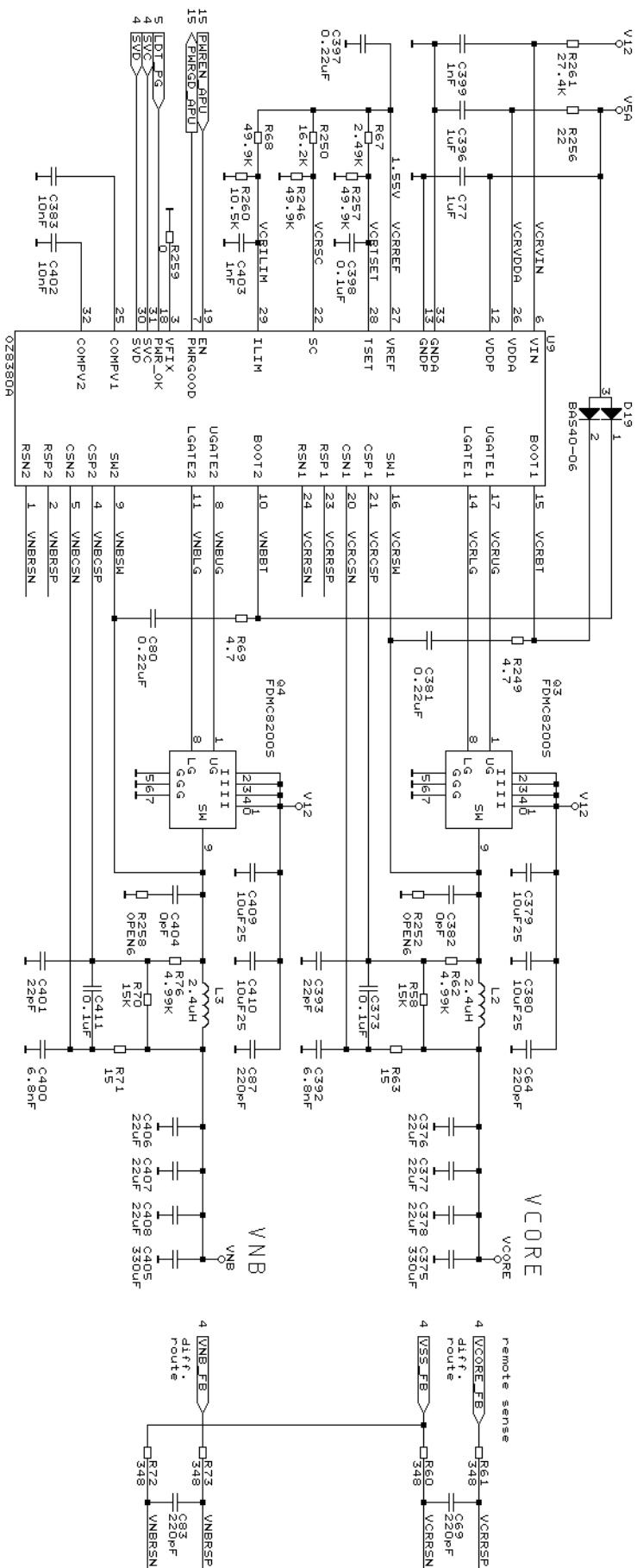


VMEM converter and VTT LDO



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Title	1.8V, 1.1V, VMEM, VTT
Size	Document Number
B	apu
Date:	May 18, 2014 Sheet 17 of 18

VCORE and VNB converter



1.05V, 2.5A (CPU)

